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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,453	03/19/2004	Ahmad H. Atriss	SC13166TC	7270

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FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
NGUYEN, KHAI M	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

Office Action Summary	Application No.	Applicant(s)	
	10/804,453	ATRISS ET AL.	
	Examiner	Art Unit	
	Khai M. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/19/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 5, 10-13, 17-25, 36-44, and 46* is/are rejected.

7)☒ Claim(s) *3-4, 6-9, 14-16, 26-35, 45, and 47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-19-2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-2 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The phrase "at least one of the analog input signal" in claims 1-2 and the phrase "at least one of the analog signal input node" in claim 23 are unclear to the examiner and/or lack of antecedent basis – therefore, the claims are indefinite. Correction/clarification is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 5, 10-13, 17-25, 36-44, and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Garrity et al. (US 5,574,457) (or **Garrity**).

Regarding claim 1, Garrity discloses an ADC (Fig. 2), comprising: an amplifier (22) having an input coupled to node 25 and an output coupled to Vout; and a switched capacitor network (C1...C4) coupled to the input of the amplifier and being coupled to receive an analog input signal (Vin) and a plurality of reference input signals (VREFP, VREFM) input to the ADC, the switched capacitor network comprising a plurality of

capacitors and switches (C1...C4, and S1...S10), each of the plurality of capacitors being coupled to receive at least one of the analog input signal (Vin) or the reference input signals (VREFP, VREFM), wherein the amplifier and switched capacitor network (C1...C4) are configured to scale at least one of the plurality of reference input signals (either VREFP or VREFM) by a predetermined scale factor, the predetermined scale factor being determined at least in part by capacitance values (column 4, lines 46-54 and column 5, lines 5-16) of the switched capacitor network, the amplifier and switched capacitor network being further configured to provide an output signal (Vout) comprising a predetermined gain (two, for example, column 4, lines 45+) of the analog input signal adjusted by the predetermined scale factor of the at least one of the plurality of reference input signals.

Regarding claim 2, Garrity discloses the ADC of claim 1 including: two reference input signals (VREFP/VREFM), and the switched capacitor network comprising: a first capacitor (C1) controllably coupled (by one of the switches) to receive the analog input signal (when S2 is closed), a second capacitor (C2) controllably coupled (by another switch from S1...S12) to alternately receive the analog input signal (Vin) or the first reference input signal (VREFM); and a third capacitor (C4) controllably coupled (by switches S11-S12) to receive at least one signal of the analog input signal (Vin – when S11 is closed) or the second reference input signal (VREFP – when S12 is closed).

Regarding claim 5, Garrity discloses the capacitances of the second/third capacitors are substantially equal (col. 4, lines 45-46 and col. 5, lines 6-8).

Regarding claim 10, Garrity discloses the first capacitor (C1) is controllably coupled (when S1 is closed) to receive a feedback signal from the output of the amplifier (22 – Fig. 2).

Regarding claims 11-12, Garrity discloses the reference signals of the above claims are power supply/ground signals (Fig. 2).

Regarding claim 13, Garrity discloses the third capacitor is further controllably coupled to one of the reference input signal but not connected to the analog input signal, and wherein the first capacitor (C1) and the second capacitor (C2) are coupled to the analog input signal (V1) during a first clock phase (CLK1) and the second capacitor is coupled to the first reference input signal (VREFM) during a second clock phase (CLK1BAR).

Regarding claim 17, Garrity discloses that the predetermined scaled factor of the above claims is selectable (adding/subtracting from the output voltage – column 2, lines 53-55 and column 3, lines 33-67) after the power is provided to the integrated circuit, the predetermined scale factor being selectable from a range of scale factors including a scale factor of one.

Regarding claims 18-19, Garrity discloses the apparatus of the above claims including at least one RSD stage (the cascaded or serially connected gain stages of Fig. 1), each of the gain stages comprising a respective amplifier (22 – Fig. 2) and a switch capacitor network (S1-S12 and C1-C4).

Regarding claim 20, Garrity discloses the apparatus of the above claims is a cyclic ADC and wherein each ADC stage is a redundant signed digit stage (because it

comprises sample/hold circuits and more than one stages as seen in Figs. 1-2 and the text).

Regarding claims 21-22, Garrity discloses the apparatus of the above claims (Figs. 1-2 and 8) including a plurality of MDAC (inside the gain stages – the gain stages having a gain of two - column 2, lines 53-55), each of the ADC stages (12) including a respective one of the plurality of MDACs (Fig. 2), each of the plurality of MDACs including a respective amplifier (22) and switched capacitor network (S1-S12 and C1-C4).

Regarding claim 23, Garrity discloses an ADC, a processing and scaling circuit comprising: an amplifier (22 – Fig. 2) comprising an input (inverting/non-inverting) and an output (Vout), the amplifier having operational range within a power supply range; and a switched capacitor circuit (C1...C4) coupled to the input of the amplifier and the output of the amplifier, the switched capacitor circuit comprising: an analog signal input node for receiving an analog signal (Vin), a reference input node for receiving a reference signal (VREFM/VREFP) capable of having a value outside the operational range of the amplifier, a plurality of capacitance elements (C1-C4), each of the plurality of capacitance elements being controllably coupled (by controlling switches S1-S12) to at least one of the analog signal input node or the reference input node and being controllably coupled to the input of the amplifier; wherein, the amplifier and switched capacitor circuit, responsive to receiving the analog signal and the reference signal, scale the reference signal (by adding/subtracting the reference signal from the output of the amplifier 22 – see column 2, lines 53-55, for example) by a predetermined scale

factor to provide a scaled reference signal within the operational range of the amplifier, and process the analog signal to provide an output signal having a predetermined gain (two for example) of the analog signal adjusted by the predetermined scale factor of the reference signal.

Regarding claim 24, Garrity discloses the ADC of claim 23 wherein the switched capacitor circuit further comprises: first, second and third capacitors (C1...C3), each having first and second terminals; a first switch (S2) coupled between the first terminal of the first capacitor and the analog signal input node; a second switch (S5) coupled between the first terminal of the second capacitor (C2) and the analog signal input node; a third switch (S6) coupled between the first terminal of the second capacitor and a first power supply signal terminal (VREFM input terminal); and a fourth switch (S12) coupled between the first terminal of the third capacitor and the reference input node.

Regarding claim 25, Garrity discloses the first and second capacitors are coupled to receive the analog signal (as seen in Figs. 4-5) and the third capacitor is not coupled to receive the analog signal (Figs. 4-5).

Regarding claim 36, Garrity discloses the switched capacitor circuit (C1-C4) comprising a feedback input node coupled to receive an amplifier feedback signal (Vout), and the first terminal of the first capacitor (C1) is controllably coupled (by controlling the on/off of the switches S1-S2) to alternately receive the analog signal and the amplifier feedback signal.

Regarding claim 37, Garrity discloses that the predetermined scaled factor of the above claims is selectable (adding/subtracting from the output voltage – column 2, lines

53-55 and column 3, lines 33-67) after the power is provided to the integrated circuit, the predetermined scale factor being selectable from a range of scale factors including a scale factor of one.

Regarding claims 38-39, Garrity discloses the reference signal is one of a plurality of reference signals (VREFM/VREFP), the reference signals comprising a maximum power potential (VREFM or VREFP) and minimum power potential (VREFP or VREFM or ground).

Regarding claim 40, Garrity discloses the reference signal is one of at least three reference signals, the at least three reference signals comprising a maximum reference signal, a minimum reference signal, and middle reference signal, the middle reference signal being at a potential between potentials of the maximum and minimum reference signals (see Fig. 8).

Regarding claim 41, Garrity discloses the reference signal is one of a plurality of reference signals, the plurality of reference signals comprising first and second voltage signals (VREFP/VREFM) configured for derivation from a bandgap voltage (Vout).

Regarding claim 42, Garrity discloses the apparatus of the above claims is configured to receive first and second power supply signals, and the reference signal is one of the first and second power supply signals (Fig. 2 and Fig. 8).

Regarding claim 43, Garrity discloses a method for processing an analog signal, comprising: receiving an analog signal (Vin – the input signal) at an analog-to-digital conversion (ADC) stage (Figs. 1-2); receiving an unscaled reference signal (VREFM/VREFP) at the ADC stage; generating a scaled reference signal from the

unscaled reference signal by a switched capacitance and amplification circuit of the ADC stage (that is adjusting accordingly from the output voltage – see column 2, lines 53-55 and column 3, lines 33+); and generating and outputting a processed signal (Vout) from the analog signal and the scaled reference signal by alternately coupling the analog signal and unscaled reference (VREFM/VREFP) signal to capacitors (C1...C4) of the switched capacitance and amplification circuit.

Regarding claim 44, Garrity discloses a method associated with the apparatus of the above claims, wherein the method comprising: receiving an input signal (Vin) having a first operating range of voltages; receiving a reference potential (Vrefm,p); providing the input signal and the reference potential to a switched capacitor network comprising switched capacitors (C1-C4 and switch S1-S12) and an amplifier (22); scaling (by either subtracting/adding – see column 3, lines 33+) the reference potential by a predetermined scale factor determined by capacitive values (column 4, lines 45-67) within the switched capacitor network to provide a scaled reference signal within a second operating range of voltages; and processing the input signal also with the switched capacitor network to provide an output signal comprising a predetermined gain of the input signal adjusted by the scaled reference signal.

Regarding claim 46, Garrity teaches the method including a step of converting the analog signal (the input signal) to the digital signal (the output signal – Fig. 1) using the scaled reference signal (by either subtracting/adding – see column 3, lines 33+).

Allowable Subject Matter

4. Claims 3-4, 6-9, 14-16, 26-35, 45, and 47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 8:00 to 4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KN
February 14, 2005

Michael Tokar
Supervisory Patent Examiner
Technology Center 2800